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NB3N3020DTR2G

onsemi

Phase Locked Loops - PLL LVPECL CLK MULTIPLR 3.3V

Any questions, please feel free to contact us.
info@kaimte.com

NB3N3020

3.3 V, LVPECL/LVCMOS Clock Multiplier

Description

The NB3N3020 is a high precision, low phase noise selectable clock multiplier. The device takes a 5 – 27 MHz fundamental mode parallel resonant crystal or a 2 – 210 MHz LVCMOS single ended clock source and generates a differential LVPECL output and a single ended LVCMOS/LVTTL output at a selectable clock output frequency which is a multiple of the input clock frequency. Three tri-level (Low, Mid, High) LVCMOS/LVTTL single ended select pins set one of 26 possible clock multipliers. The LVCMOS/LVTTL output enable (OE1) tri-states the LVCMOS/LVTTL clock output (CLK1) when low. When the LVTTL/LVCMOS output enable (OE2) is LOW, LVPECL CLK2 is forced LOW and LVPECL $\overline{\text{CLK2}}$ is forced HIGH.

This device is housed in 5 mm x 4.4 mm narrow body TSSOP 16 pin package.

Features

- Selectable Clock Multiplier
- External Loop Filter is Not Required
- LVPECL Differential Output
- LVCMOS/ LVTTL Outputs
- RMS Period Jitter of 5 ps
- Jitter or Low Phase Noise at 125 MHz [25 MHz Input]:

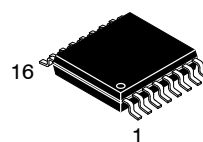
| Offset | Noise Power |
|---------|-------------|
| 100 Hz | -95 dBc/Hz |
| 1 kHz | -107 dBc/Hz |
| 10 kHz | -112 dBc/Hz |
| 100 kHz | -117 dBc/Hz |
| 1 MHz | -117 dBc/Hz |
| 10 MHz | -134 dBc/Hz |

- Operating Range 3.3 V \pm 10%
- Industrial Temperature Range -40°C to +85°C
- These are Pb-Free Devices



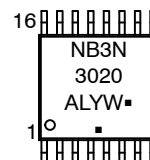
ON Semiconductor®

<http://onsemi.com>



TSSOP-16
DT SUFFIX
CASE 948F

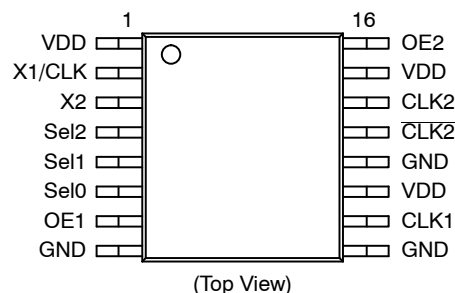
MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(*Note: Microdot may be in either location)

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NB3N3020

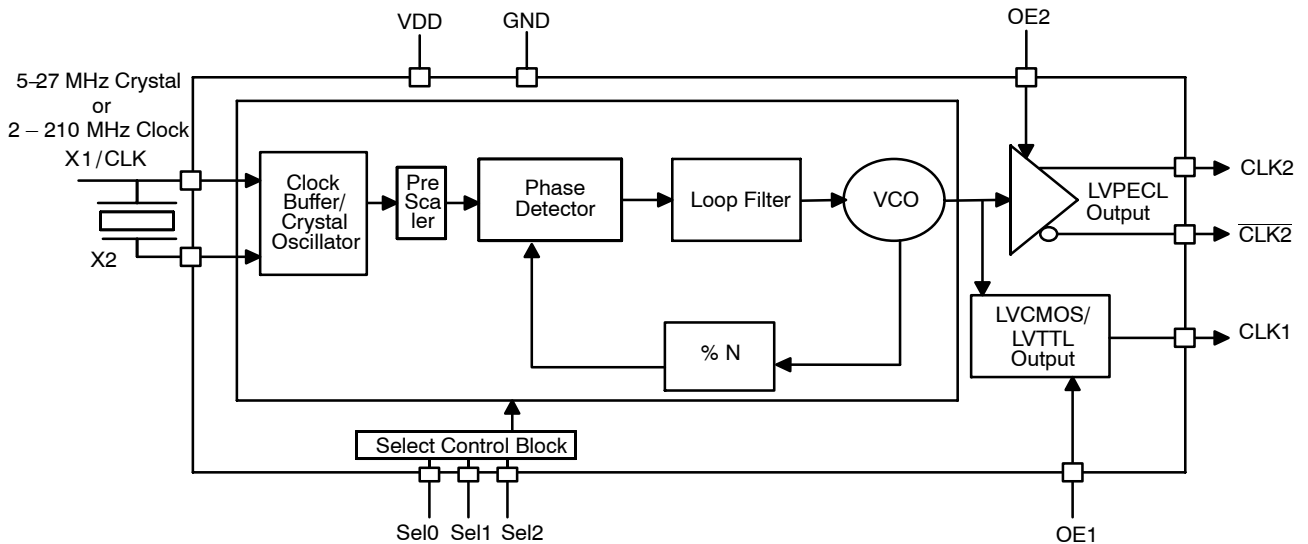


Figure 1. NB3N3020 Simplified Logic Diagram

Table 1. PIN DESCRIPTION

| Pin | Name | I/O | Description |
|-----------|-----------------|----------------------|---|
| 6 | Sel0 | Tri-Level Input | Frequency select input 0. When left open, defaults to VDD/ 2. See output select Table 2 for details. |
| 5 | Sel1 | Tri-Level Input | Frequency select input 1. When left open, defaults to VDD/ 2. See output select Table 2 for details. |
| 4 | Sel2 | Tri-Level Input | Frequency select input 2. When left open, defaults to VDD/ 2. See output select Table 2 for details. |
| 1, 11, 15 | V _{DD} | Power Supply | Positive supply voltage pins are connected to +3.3 V supply voltage. |
| 2 | X1/CLK | Input | Crystal or Clock input. Connect to 5 – 27 MHz crystal source or 2 – 210 MHz single-ended clock. See Table 2. |
| 3 | X2 | Input | Crystal input. Connect to a 5 – 27 MHz crystal or leave unconnected for clock input. See Table 2. |
| 7 | OE1 | LVTTL/LVCMOS Input | Output enable input that synchronously tri-states CLK1 output when low. Internal pull-up resistor to V _{DD} . |
| 16 | OE2 | LVTTL/LVCMOS Input | Output enable input that when LOW synchronously controls LVPECL outputs by forcing CLK2 LOW and CLK2 HIGH. Internal pull-up resistor to V _{DD} . |
| 8, 9, 12 | GND | Power Supply | Ground 0 V. These pins provide GND return path for the devices. |
| 13 | CLK2 | LVPECL Output | Inverted clock output. Clock frequency equals input frequency times multiplier. |
| 14 | CLK2 | LVPECL Output | Non-inverted clock output. Clock frequency equals input frequency times multiplier. |
| 10 | CLK1 | LVTTL/ LVCMOS Output | Clock Output. Clock frequency equals input frequency times multiplier. |

NB3N3020

Table 2. OUTPUT FREQUENCY CLOCK MULTIPLIER SELECT TABLE

| Sel2 | Sel1 | Sel0 | CLK1, CLK2, $\overline{\text{CLK2}}$ | Clock Input Range [MHz] | Crystal Input Range [MHz] |
|------|------|------|--------------------------------------|-------------------------|---------------------------|
| L | L | L | Low (Power Down) | – | – |
| L | L | M | Input X 1 | 25 – 210 | 25 – 27 |
| L | L | H | Input X 4/3 (or 1 1/3) | 15 – 157.5 | 15 – 27 |
| L | M | L | Input X 1.5 | 10 – 140 | 10 – 27 |
| L | M | M | 1.6 | 25 – 131.25 | 25 – 27 |
| L | M | H | Input X 1.875 | 40 – 112 | – |
| L | H | L | Input X 2 | 25 – 105 | 25 – 27 |
| L | H | M | Input X 7/3 (or 2 1/3) | 15 – 90 | 15 – 27 |
| L | H | H | Input X 2.4 | 25 – 87.5 | 25 – 27 |
| M | L | L | Input X 2.5 | 10 – 84 | 10 – 27 |
| M | L | M | Input X 8/3 (or 2 2/3) | 15 – 78.75 | 15 – 27 |
| M | L | H | Input X 3 | 15 – 70 | 15 – 27 |
| M | M | L | Input X 3.125 | 40 – 67.20 | – |
| M | M | M | Input X 3.2 | 25 – 65.63 | 25 – 27 |
| M | M | H | Input X 10/3 (or 3 1/3) | 15 – 63 | 15 – 27 |
| M | H | L | Input X 3.75 | 20 – 56 | 20 – 27 |
| M | H | M | Input X 4 | 2 – 52.5 | 5 – 25 |
| M | H | H | Input X 5 | 6 – 42 | 6 – 27 |
| H | L | L | Input X 6 | 5 – 35 | 5 – 27 |
| H | L | M | Input X 6.25 | 20 – 33.6 | 20 – 27 |
| H | L | H | Input X 19/3 (or 6 1/3) | 15 – 33.16 | 15 – 27 |
| H | M | L | Input X 8 | 5 – 26.25 | 5 – 26.25 |
| H | M | M | Input X 25/3 (or 8 1/3) | 15 – 25.2 | 15 – 25.2 |
| H | M | H | Input X 10 | 5 – 21 | 5 – 21 |
| H | H | L | Input X 12 | 5 – 17.5 | 5 – 17.5 |
| H | H | M | Input X 12.5 | 10 – 16.8 | 10 – 16.8 |
| H | H | H | Input X 16 | 5 – 13.125 | 5 – 13.125 |

L – Low, M – Mid, H – High

Recommended Crystal Parameters

| | |
|------------------------------|--------------------|
| Crystal | Fundamental AT–Cut |
| Frequency | 5 – 27 MHz |
| Load Capacitance | 16 – 20 pF |
| Shunt Capacitance, C0 | 7 pF Max |
| Equivalent Series Resistance | 35 Ω Max |
| Initial Accuracy at 25°C | ± 20 ppm |
| Temperature Stability | ± 30 ppm |
| Aging | ± 20 ppm |
| C0/C1 Ration | 250 Max |

Device Operation

The NB3N3020 is a Clock multiplier. The device can take crystal or clock input and generates LVPECL and LVCMOS/ LVTTTL clock outputs which are multiples of the

input as determined by the tri–level select inputs [Sel0, Sel1, Sel2].

Clock Multiplication

NB3N3020 is a clock multiplier with the clock multiplier selected by the tri level select inputs [Sel0, Sel1, Sel2]. NB3N3020 has a LVTTTL/LVCMOS output [CLK1] and a LVPECL clock output [CLK2, $\overline{\text{CLK2}}$].

Output Enable

The device has an output enable [OE] which is used to tri–state the outputs. OE1 controls the CLK1 clock output where as OE2 controls the CLK2, $\overline{\text{CLK2}}$ clock outputs. When OE1 or OE2 are disabled, the respective clock output(s) are tri–stated. In this mode of operation, PLL is still running, with the respective clock outputs tri–stated. When the OE1 or OE2 are enabled, the clock outputs

become active synchronous to the internal PLL output clock and do not create any glitches or runt pulses during the transition. In power down mode, the outputs are tri-stated regardless of the state of the OE1, OE2.

The device has an output enable [OE1] which accepts LVTTTL/LVCMOS levels and when set LOW will disable the LVTTTL/LVCMOS level CLK1 to tri-state. Output enable OE2 accepts LVTTTL/LVCMOS levels to disable the LVPECL level outputs by forcing CLK2 LOW and CLK2b HIGH. When OE1 or OE2 are set LOW (Disabled), the PLL remains running while the respective clock outputs are disabled. When the OE1 or OE2 are set enabled (HIGH), the clock outputs become active synchronous to the internal PLL output clock and will not create any glitches or runt pulses during the transition. Both OE1 and OE2 inputs have pull-up resistors which default to VDD when floated open. In power down mode, the outputs are tri-stated (zero current) regardless of the state of the OE1, OE2.

Changing Clock Multiplier

The clock output frequency can be dynamically changed using Sel0, Sel1, Sel2 pins. When the clock frequency is changed, the clock outputs move from one frequency to another and the PLL locks to the new frequency within a settling time of 3 msec. There is no glitch during this transition when the clock outputs are active {not tri-stated by OE1, OE2}.

Crystal/ Clock Input

The device takes in a 5 – 27 MHz crystal input or 2 – 210 MHz clock input. Once powered up, the input frequency is fixed and should not be changed dynamically. The input cannot accept a spread spectrum clock and needs a fixed frequency clock for device operation. The input frequencies for clock and crystal input for specific multipliers are determined by Table 3.

Power Up

When the NB3N3020 is powered up, it takes 10 msec for the PLL's to stabilize and lock to the desired frequency of operation as selected by Sel0, Sel1, Sel2. During this time period, there may be glitches in the clock outputs.

Power Down:

The device can be powered down when the Sel0, Sel1, Sel2 pins are all connected to GND. In this mode of operation, PLL is turned off and the device consumes less than 5 mA of current. There may be a glitch in clock outputs when the device is powering down. In power down mode, the outputs are tri-stated regardless of the state of the OE1, OE2.

In the cases where the application requires glitch-less transitions, in order to avoid glitches it is recommended to use synchronous OE signaling to mask glitches to the clock outputs.

NB3N3020

Table 3. ATTRIBUTES

| Characteristics | Value |
|--|----------------------|
| ESD Protection Human Body Model | 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Dry pack (Note 1) | Level 1 |
| Flammability Rating Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | 8287 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 2)

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---------------|--|--------------------|----------------------------|----------------------------|------|
| V_{DD} | Positive Power Supply | GND = 0 V | | 4.6 | V |
| V_I | Input Voltage (VIN) | GND = 0 V | $GND \leq V_I \leq V_{DD}$ | -0.5 V to $V_{DD} + 0.5$ V | V |
| I_{out} | LVPECL Output Current | Continuous Surge | | 25 50 | mA |
| T_A | Operating Temperature Range | | | -40 to +85 | °C |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | TSSOP-16 TSSOP-16 | 138 108 | °C/W |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | (Note 3) | TSSOP-16 | 33 to 36 | °C/W |
| T_{sol} | Wave Solder | | | 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
- JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 5. DC CHARACTERISTICS ($V_{DD} = 3.3$ V $\pm 10\%$, GND = 0 V, $T_A = -40$ °C to +85°C)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|-------------|--|------------------|------------|------------------|------|
| V_{DD} | Power Supply Voltage | 2.97 | 3.3 | 3.63 | V |
| I_{DD} | Power Supply Current (Note 4) | | 60 | 75 | mA |
| I_{DDOE} | Power Supply Current when OE1, OE2 is Set Low | | 50 | | mA |
| I_{DDOFF} | Power Supply Current when PLL is powered off by Sel0, Sel1, Sel2 | | | 5 | mA |
| V_{IH} | Input HIGH Voltage (X1/CLK, OE1, OE2) | 2000 | | $V_{DD} + 300$ | mV |
| V_{IL} | Input LOW Voltage (X1/ \overline{CLK} , OE1, OE2) | GND - 300 | | 800 | mV |
| V_{IH} | Input HIGH Voltage (Sel0, Sel1, Sel2) | 0.72 V_{DD} | | $V_{DD} + 300$ | mV |
| V_{IL} | Input LOW Voltage (Sel0, Sel1, Sel2) | GND - 300 | | 800 | mV |
| V_{IM} | Input Mid Voltage (Sel0, Sel1, Sel2) (When left open, defaults to $V_{DD}/2$) | | $V_{DD}/2$ | | mV |
| V_{OH} | Output HIGH Voltage for CLK2, $\overline{CLK2}$ (See Figure 3) | $V_{DD} - 1.145$ | | $V_{DD} - 0.895$ | V |
| V_{OL} | Output LOW Voltage for CLK2, $\overline{CLK2}$ (See Figure 3) | $V_{DD} - 2.090$ | | $V_{DD} - 1.600$ | V |
| V_{OH} | Output HIGH Voltage for CLK1 [$I_{OH} = -12$ mA] | 2.4 | | | V |
| V_{OL} | Output LOW Voltage for CLK1 [$I_{OL} = 12$ mA] | | | 0.4 | V |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Measurement taken at $f_{CLK_{out}} = 125$ MHz with LVPECL and LVCMOS/ LVTTTL outputs not terminated.

NB3N3020

Table 6. AC CHARACTERISTICS ($V_{DD} = 3.3 \text{ V} \pm 10\%$, $GND = 0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) (Note 5)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|-------------------|---|-----|------|------|--------|
| f_{CLKIN} | Crystal Input Frequency | 5.0 | | 27 | MHz |
| f_{CLKIN} | Clock Input Frequency | 2.0 | | 210 | MHz |
| f_{CLKOUT} | Output Clock Frequency | | | 210 | MHz |
| Φ_{NOISE} | Phase-Noise Performance ($f_{CLKout} = 125 \text{ MHz}$, 25 MHz input) | | | | |
| | @ 100 Hz offset from carrier | | -95 | | dBc/Hz |
| | @ 1 kHz offset from carrier | | -107 | | dBc/Hz |
| | @ 10 kHz offset from carrier | | -112 | | dBc/Hz |
| | @ 100 kHz offset from carrier | | -117 | | dBc/Hz |
| | @ 1 MHz offset from carrier | | -117 | | dBc/Hz |
| | @ 10 MHz offset from carrier | | -134 | | dBc/Hz |
| Tjitter p-p | Cycle-to-Cycle Jitter peak to peak (Note 6) $f_{CLKout} = 100 \text{ MHz}$ and 125 MHz, 25 MHz input | | 20 | 36 | ps |
| Tjitter rms | Cycle-to-Cycle Jitter rms (Note 7) $f_{CLKout} = 100 \text{ MHz}$ and 125 MHz, 25 MHz input | | 5.0 | 9.0 | ps |
| Tjitter p-p | Period Jitter peak to peak (Note 7) $f_{CLKout} = 100 \text{ MHz}$ and 125 MHz, 25 MHz input | | 15 | 20 | ps |
| Tjitter rms | Period Jitter rms (Note 7) $f_{CLKout} = 100 \text{ MHz}$ and 125 MHz, 25 MHz input | | 3.0 | 5.0 | ps |
| | Start up time from power up | | 10 | | ms |
| OE | Output Enable/Disable Time | | 10 | | us |
| | PLL settling time | | 3 | | ms |
| t_{DUTY_CYCLE} | Output Clock Duty Cycle (Measured at cross point for LV PECL clock output and $V_{DD}/2$ for LVCMOS/ LVTTTL clock output) | 45 | 50 | 55 | % |
| t_R | Output Rise Time (Note 5) (Measured from 20% to 80%. Figure 2) LV PECL Output | | 340 | 700 | ps |
| t_F | Output Fall Time (Note 5) (Measured from 20% to 80%. Figure 2) LV PECL Output | | 340 | 700 | ps |
| t_R | Output Rise Time (Measured from 0.8 to 2 V, no load) LVCMOS/ LV TTL Output | | | 1500 | ps |
| t_F | Output Fall Time (Measured from 2.0 V to 0.8 V, no load) LVCMOS/ LV TTL Output | | | 1500 | ps |
| t_R/ t_F | Input Rise time/ Fall time for LV CMOS/ LV TTL clock input [X1/CLK] | 0 | | 1500 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Measurement taken with outputs terminated with 50Ω to $V_{DD} - 2 \text{ V}$. See Figure 2.

6. Sampled with 1000 cycles

7. Sampled with 10000 cycles

NB3N3020

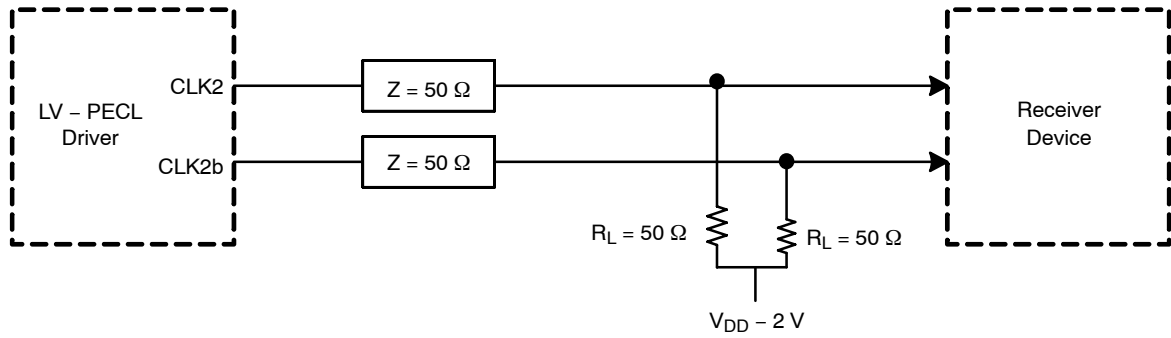


Figure 2. Typical Termination for Output Driver for Device Evaluation

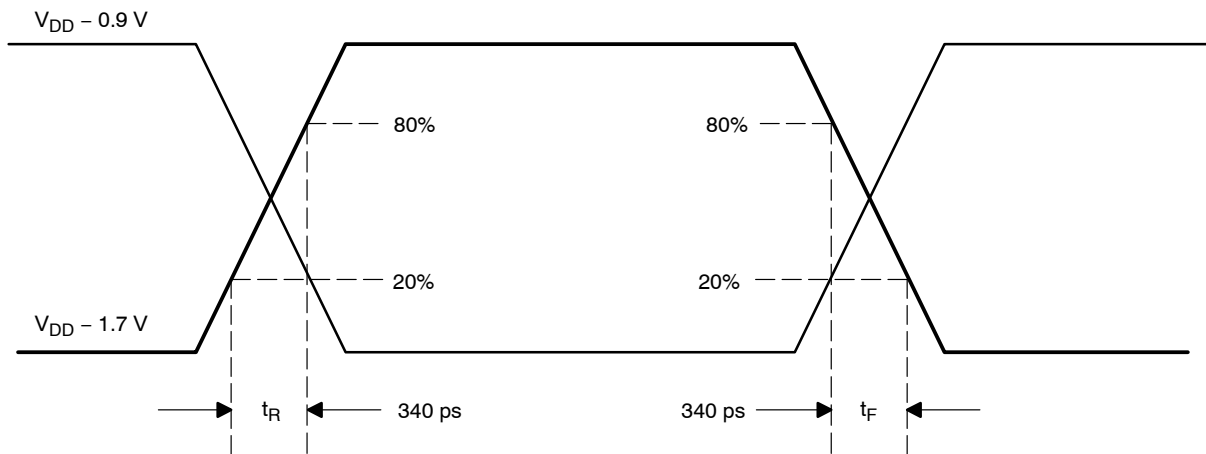


Figure 3. LV-PECL Output Parameter Characteristics

ORDERING INFORMATION

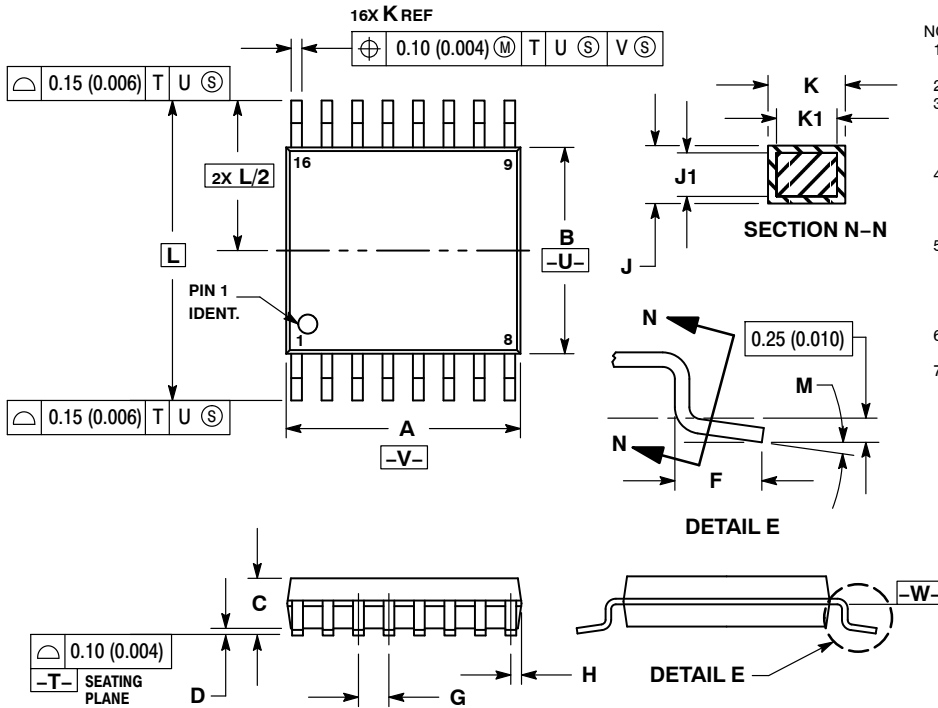
| Device | Package | Shipping [†] |
|---------------|-----------------------|-----------------------|
| NB3N3020DTG | TSSOP-16 (Pb-Free) | 96 Units / Rail |
| NB3N3020DTR2G | TSSOP-16 (Pb-Free) | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB3N3020

PACKAGE DIMENSIONS

TSSOP-16
CASE 948F
ISSUE B

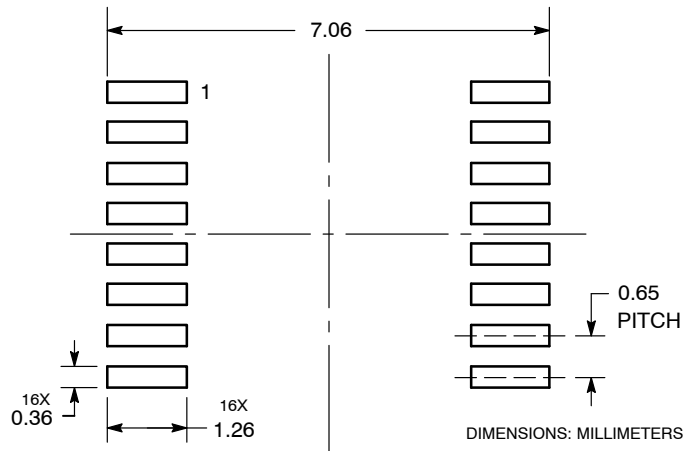


NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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