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AK5357ET-E2

AKM Semiconductor Inc.

24Bit 96kHz $\Delta\Sigma$ ADC

Any questions, please feel free to contact us.
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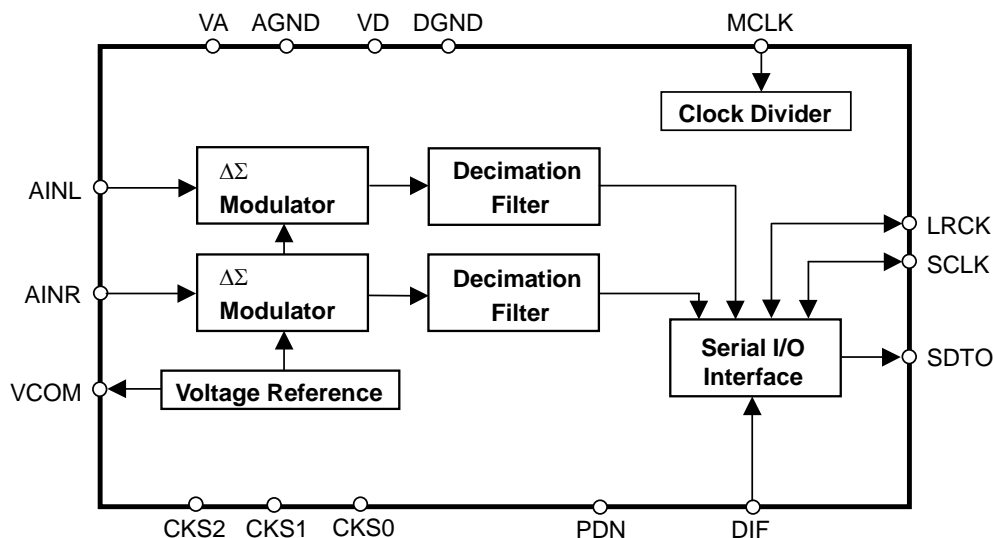
AK5357
24Bit 96kHz $\Delta\Sigma$ ADC

GENERAL DESCRIPTION

The AK5357 is a stereo A/D Converter with wide sampling rate of 4kHz ~ 96kHz and is suitable for multimedia audio system. The AK5357 achieves high accuracy and low cost by using Enhanced dual bit $\Delta\Sigma$ techniques. The AK5357 requires no external components because the analog inputs are single-ended. The audio interface has two formats (MSB justified, I²S) and can correspond to many systems like Karaoke, surround.

FEATURES

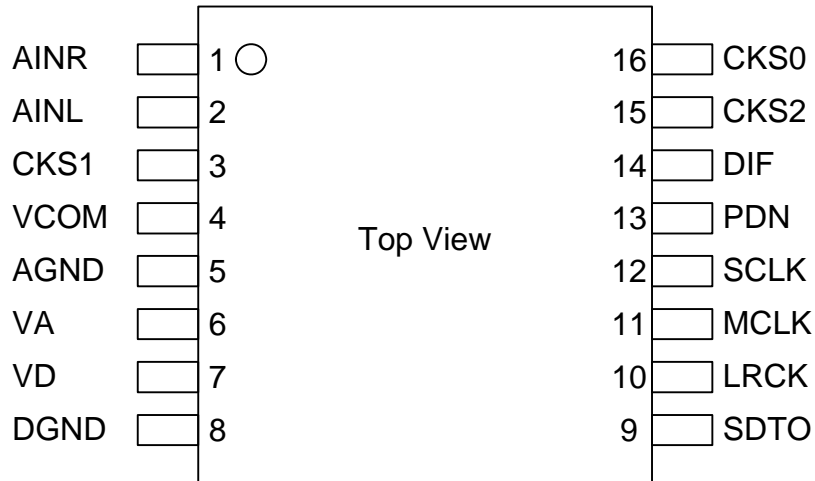
- Stereo $\Delta\Sigma$ ADC
- On-Chip Digital Anti-Alias Filtering
- Single-ended Input
- Digital HPF for DC-Offset cancel
- S/(N+D): 88dB@5V, 86dB@3V for 48kHz
- DR: 102dB@5V, 100dB@3V for 48kHz
- S/N: 102dB@5V, 100dB@3V for 48kHz
- Sampling Rate Ranging from 4kHz to 96kHz
- Master Clock:
 - 256fs/384fs/512fs/768fs (4kHz ~ 48kHz)
 - 256fs/384fs (48kHz ~ 96kHz)
- Input level: TTL/CMOS selectable
- Master / Slave Mode
- Audio Interface: 24bit MSB justified / I²S selectable
- Power Supply: 2.7 ~ 5.5V
- Ta = -20 ~ 85°C (ET), -40 ~ 85°C (VT), -40 ~ 105°C (KT)
- Small 16pin TSSOP Package
- AK5381 Pin-compatible



■ Ordering Guide

| | | |
|----------|-----------------------------|----------------------------|
| AK5357ET | -20 ~ +85°C | 16pin TSSOP (0.65mm pitch) |
| AK5357VT | -40 ~ +85°C | 16pin TSSOP (0.65mm pitch) |
| AK5357KT | -40 ~ +105°C | 16pin TSSOP (0.65mm pitch) |
| AKD5357 | Evaluation Board for AK5357 | |

■ Pin Layout



■ Compatibility with AK5353 and AK5381

| | AK5353 | AK5381 | AK5357 |
|---------------------|--|-------------------------|-------------------------|
| S/(N+D) | 84dB | 96dB | 88dB |
| DR | 96dB | 106dB | 102dB |
| Master Mode | Not Available | Available | Available |
| HPF OFF | Not Available | Available | Available |
| TTL Level Mode | 4kHz to 96kHz | 4kHz to 48kHz | 4kHz to 96kHz |
| VIH@TTL Level Mode | 2.2V | 2.4V | 2.2V |
| VA (Analog Supply) | 2.7 to 5.5V@fs=48kHz 4.5 to 5.5V@fs=96kHz | 4.5 to 5.5V@fs=48/96kHz | 2.7 to 5.5V@fs=48/96kHz |
| VD (Digital Supply) | 4.5 to 5.5V@fs=96kHz | 3.0 to 5.5V@fs=96kHz | 2.7 to 5.5V@fs=96kHz |
| Pin #3 | VREF | CKS1 | CKS1 |
| Pin #15 | TTL | CKS2 | CKS2 |
| Pin #16 | TST | CKS0 | CKS0 |

| PIN / FUNCTION | | | |
|----------------|----------|-----|--|
| No. | Pin Name | I/O | Function |
| 1 | AINR | I | Rch Analog Input Pin |
| 2 | AINL | I | Lch Analog Input Pin |
| 3 | CKS1 | I | Mode Select 1 Pin |
| 4 | VCOM | O | Common Voltage Output Pin, VA/2 Bias voltage of ADC input. |
| 5 | AGND | - | Analog Ground Pin |
| 6 | VA | - | Analog Power Supply Pin, 2.7 ~ 5.5V |
| 7 | VD | - | Digital Power Supply Pin, 2.7 ~ 5.5V |
| 8 | DGND | - | Digital Ground Pin |
| 9 | SDTO | O | Audio Serial Data Output Pin “L” Output at Power-down mode. |
| 10 | LRCK | I/O | Output Channel Clock Pin “L” Output in Master Mode at Power-down mode. |
| 11 | MCLK | I | Master Clock Input Pin |
| 12 | SCLK | I/O | Audio Serial Data Clock Pin “L” Output in Master Mode at Power-down mode. |
| 13 | PDN | I | Power Down Mode Pin “H”: Power up, “L”: Power down |
| 14 | DIF | I | Audio Interface Format Pin “H” : 24bit I ² S Compatible, “L” : 24bit MSB justified |
| 15 | CKS2 | I | Mode Select 2 Pin |
| 16 | CKS0 | I | Mode Select 0 Pin |

Note: All digital input pins should not be left floating.

■ Handling of Unused Pin

The unused input pins should be processed appropriately as below.

| Classification | Pin Name | Setting |
|----------------|----------|--------------------------|
| Analog | AINL | This pin should be open. |
| | AINR | This pin should be open. |

ABSOLUTE MAXIMUM RATINGS

 (AGND=DGND=0V; [Note 1](#))

| Parameter | | Symbol | min | max | Units |
|--|---------------------------------------|--------|------|--------|-------|
| Power Supplies: | Analog | VA | -0.3 | 6.0 | V |
| | Digital | VD | -0.3 | 6.0 | V |
| | AGND – DGND (Note 1) | ΔGND | - | 0.3 | V |
| Input Current, Any Pin Except Supplies | | IIN | - | ±10 | mA |
| Analog Input Voltage (AINL, AINR, CKS1 pins) | | VINA | -0.3 | VA+0.3 | V |
| Digital Input Voltage (All digital input pins except CKS1 pin) | | VIND | -0.3 | VD+0.3 | V |
| Ambient Temperature (powered applied) | AK5357ET | Ta | -20 | 85 | °C |
| | AK5357VT | Ta | -40 | 85 | °C |
| | AK5357KT | Ta | -40 | 105 | °C |
| Storage Temperature | | Tstg | -65 | 150 | °C |

Note 1. All voltages with respect to ground.

Note 2. AGND and DGND must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

 (AGND=DGND=0V; [Note 1](#))

| Parameter | | Symbol | min | typ | max | Units |
|--|---------|--------|-----|-----|-----|-------|
| Power Supplies (Note 3) | Analog | VA | 2.7 | 5.0 | 5.5 | V |
| | Digital | VD | 2.7 | 5.0 | VA | V |

Note 1. All voltages with respect to ground.

Note 3. The power up sequence between VA and VD is not critical.

WARNING: AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VA=VD=5.0V; AGND=DGND=0V; fs=48kHz, 96kHz; SCLK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz at fs=48kHz, 40Hz ~ 40kHz at fs=96kHz; unless otherwise specified)

| Parameter | | | min | typ | max | Units | |
|--|------------|----------------------|----------|------|-----|--------|------------|
| ADC Analog Input Characteristics: | | | | | | | |
| Resolution | | | | | 24 | Bits | |
| Input Voltage (Note 4) | VA=5V | fs=48kHz | AK5357ET | 2.7 | 3.0 | 3.3 | Vpp Vpp |
| | | | AK5357VT | 2.85 | 3.0 | 3.15 | |
| | | | fs=96kHz | 2.7 | 3.0 | 3.3 | |
| | VA=3V | | | - | 1.8 | - | Vpp |
| S/(N+D) (-1dBFS) | VA=5V | fs=48kHz | 78 | 88 | | dB | |
| | | fs=96kHz | - | 86 | | dB | |
| | VA=3V | fs=48kHz | - | 86 | | dB | |
| | | fs=96kHz | - | 84 | | dB | |
| DR (-60dBFS) | VA=5V | fs=48kHz, A-weighted | 94 | 102 | | dB | |
| | | fs=96kHz | 88 | 97 | | dB | |
| | VA=3V | fs=48kHz, A-weighted | - | 100 | | dB | |
| | | fs=96kHz | - | 95 | | dB | |
| S/N | VA=5V | fs=48kHz, A-weighted | 94 | 102 | | dB | |
| | | fs=96kHz | 88 | 97 | | dB | |
| | VA=3V | fs=48kHz, A-weighted | - | 100 | | dB | |
| | | fs=96kHz | - | 95 | | dB | |
| Input Resistance | | | fs=48kHz | 13 | 20 | kΩ | |
| | | | fs=96kHz | 9 | 14 | kΩ | |
| Interchannel Isolation | | | 90 | 110 | | dB | |
| Interchannel Gain Mismatch | | | | 0.1 | 0.5 | dB | |
| Gain Drift | | | | 100 | - | ppm/°C | |
| Power Supply Rejection | (Note 5) | | - | 50 | | dB | |
| Power Supplies | | | | | | | |
| Power Supply Current | | | | | | | |
| Normal Operation (PDN pin = "H") | | | | | | | |
| VA | | | | | 11 | 17 | mA |
| VD | (fs=48kHz) | (Note 6) | | 3 | 5 | mA | |
| VD | (fs=96kHz) | (Note 7) | | 6 | 9 | mA | |
| Power down mode (PDN pin = "L") (Note 8) | | | | | | | |
| VA+VD | | | | | 10 | 100 | μA |

Note 4. This value is the full scale (0dB) of the input voltage. Input voltage is proportional to VA voltage.
 $V_{in} = 0.6 \times V_A (V_{pp})$.

Note 5. PSR is applied to VA and VD with 1kHz, 50mVpp.

Note 6. VD=2mA@3V

Note 7. VD=4mA@3V

Note 8. All digital input pins are held VD or DGND.

FILTER CHARACTERISTICS (fs=48kHz)

(Ta=Tmin ~ Tmax; VA=VD=2.7 ~ 5.5V)

| Parameter | Symbol | min | typ | max | Units | |
|---|--------|--------|-----|-------|-------|-----|
| ADC Digital Filter (Decimation LPF): | | | | | | |
| Passband (Note 9) | | ±0.1dB | PB | 0 | 18.9 | kHz |
| | | -0.2dB | | - | 20.0 | kHz |
| | | -3.0dB | | - | 23.0 | kHz |
| Stopband | SB | 28 | | | kHz | |
| Passband Ripple | PR | | | ±0.04 | dB | |
| Stopband Attenuation | SA | 68 | | | dB | |
| Group Delay Distortion | ΔGD | | 0 | | μs | |
| Group Delay (Note 10) | GD | | 16 | | 1/fs | |
| ADC Digital Filter (HPF): | | | | | | |
| Frequency Response (Note 9) | | -3dB | FR | 1.0 | | Hz |
| | | -0.1dB | | 6.5 | | Hz |

FILTER CHARACTERISTICS (fs=96kHz)

(Ta=Tmin ~ Tmax; VA=VD=2.7 ~ 5.5V)

| Parameter | Symbol | min | typ | max | Units | |
|---|--------|--------|-----|-------|-------|-----|
| ADC Digital Filter (Decimation LPF): | | | | | | |
| Passband (Note 9) | | ±0.1dB | PB | 0 | 37.8 | kHz |
| | | -0.2dB | | - | 40.0 | kHz |
| | | -3.0dB | | - | 46.0 | kHz |
| Stopband | SB | 56 | | | kHz | |
| Passband Ripple | PR | | | ±0.04 | dB | |
| Stopband Attenuation | SA | 68 | | | dB | |
| Group Delay Distortion | ΔGD | | 0 | | μs | |
| Group Delay (Note 10) | GD | | 16 | | 1/fs | |
| ADC Digital Filter (HPF): | | | | | | |
| Frequency Response (Note 9) | | -3dB | FR | 2.0 | | Hz |
| | | -0.1dB | | 13.0 | | Hz |

Note 9. The passband and stopband frequencies scale with fs.

For example, PB=18.9kHz@±0.1dB is $0.39375 \times fs$.

Note 10. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC.

DC CHARACTERISTICS (CMOS Level Mode)

(Ta=Tmin ~ Tmax; VA=VD=2.7 ~ 5.5V)

| Parameter | Symbol | min | typ | max | Units |
|---------------------------------------|--------|--------|-----|-------|-------|
| High-Level Input Voltage | VIH | 70%VD | - | - | V |
| Low-Level Input Voltage | VIL | - | - | 30%VD | V |
| High-Level Output Voltage (Iout=-1mA) | VOH | VD-0.5 | - | - | V |
| Low-Level Output Voltage (Iout=1mA) | VOL | - | - | 0.5 | V |
| Input Leakage Current | Iin | - | - | ±10 | μA |

DC CHARACTERISTICS (TTL Level Mode)

(Ta=Tmin ~ Tmax; VA=VD=4.5 ~ 5.5V)

| Parameter | Symbol | min | typ | max | Units |
|--|--------|--------|-----|-------|-------|
| High-Level Input Voltage (CKS2-0 pins) | VIH | 70%VD | - | - | V |
| (All pins except CKS2-0 pins) | VIH | 2.2 | - | - | V |
| Low-Level Input Voltage (CKS2-0 pins) | VIL | - | - | 30%VD | V |
| (All pins except CKS2-0 pins) | VIL | - | - | 0.8 | V |
| High-Level Output Voltage (Iout=-1mA) | VOH | VD-0.5 | - | - | V |
| Low-Level Output Voltage (Iout=1mA) | VOL | - | - | 0.5 | V |
| Input Leakage Current | Iin | - | - | ±10 | μA |

SWITCHING CHARACTERISTICS

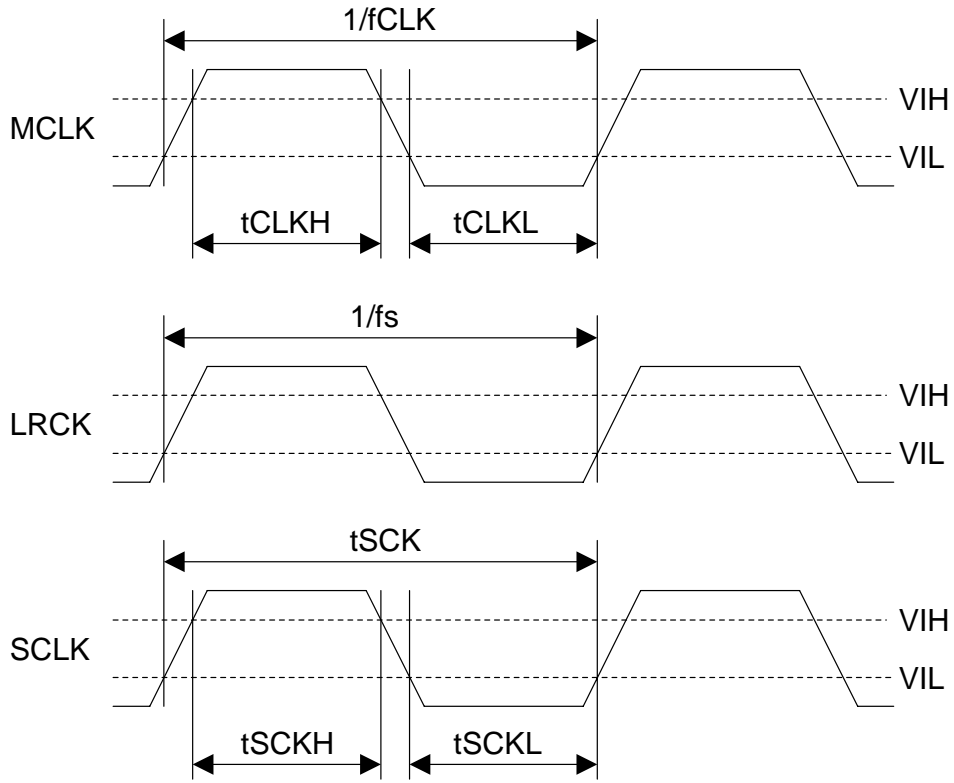
(Ta=Tmin ~ Tmax; VA=VD=2.7 ~ 5.5V; CL=20pF)

| Parameter | Symbol | min | typ | max | Units |
|---|-------------|----------|------|--------|-------|
| Master Clock Timing | | | | | |
| Frequency | fCLK | 1.024 | | 36.864 | MHz |
| Pulse Width Low | tCLKL | 0.4/fCLK | | | ns |
| Pulse Width High | tCLKH | 0.4/fCLK | | | ns |
| LRCK Frequency | | | | | |
| | fs | 4 | | 96 | kHz |
| Duty Cycle | Slave mode | 45 | | 55 | % |
| | Master mode | | 50 | | % |
| Audio Interface Timing | | | | | |
| Slave mode | | | | | |
| SCLK Period | tSCK | 160 | | | ns |
| SCLK Pulse Width Low | tSCKL | 65 | | | ns |
| Pulse Width High | tSCKH | 65 | | | ns |
| LRCK Edge to SCLK “↑” | tLRSH | 30 | | | ns |
| SCLK “↑” to LRCK Edge | tSHLR | 30 | | | ns |
| LRCK to SDTO (MSB) (Except I ² S mode) | tLRS | | | 35 | ns |
| SCLK “↓” to SDTO | tSSD | | | 35 | ns |
| Master mode | | | | | |
| SCLK Frequency | fSCK | | 64fs | | Hz |
| SCLK Duty | dSCK | | 50 | | % |
| SCLK “↓” to LRCK | tMSLR | -20 | | 20 | ns |
| SCLK “↓” to SDTO | tSSD | -20 | | 35 | ns |
| Reset Timing | | | | | |
| PDN Pulse Width | tPD | 150 | | | ns |
| PDN “↑” to SDTO valid at Slave Mode | tPDV | | 4132 | | 1/fs |
| PDN “↑” to SDTO valid at Master Mode | tPDV | | 4129 | | 1/fs |

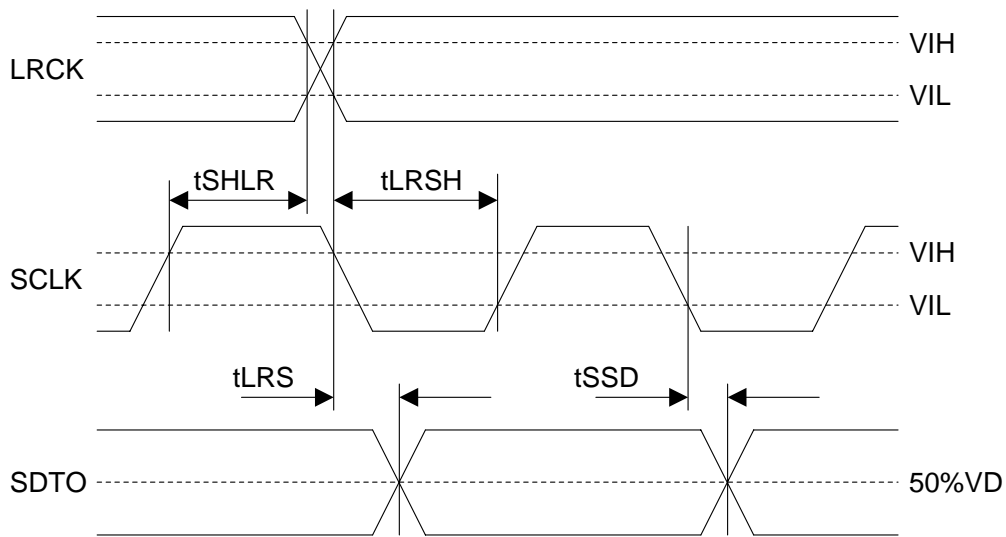
Note 11. SCLK rising edge must not occur at the same time as LRCK edge.

Note 12. The AK5357 can be reset by bringing the PDN pin = “L”.

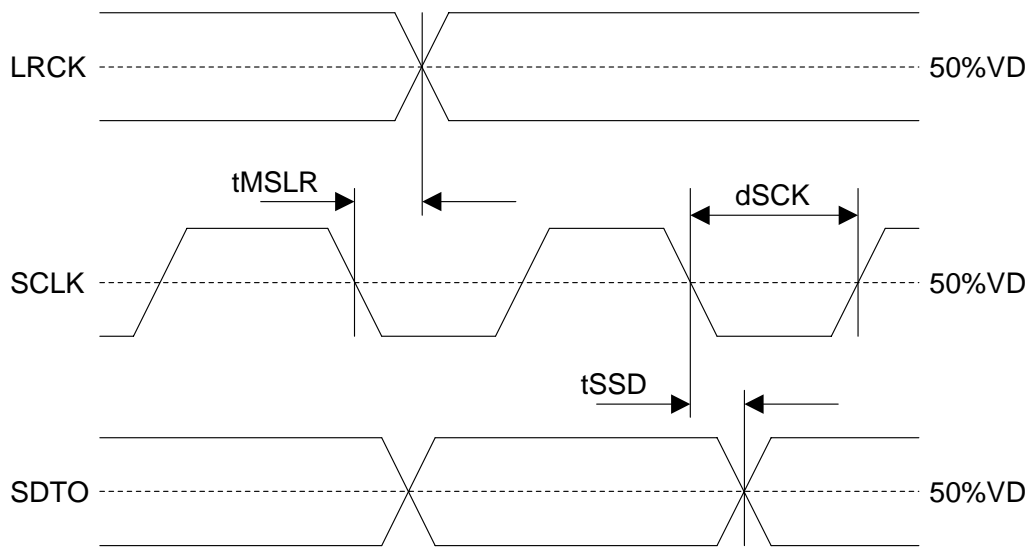
Note 13. This cycle is the number of LRCK rising edges from the PDN pin = “H”.

■ Timing Diagram


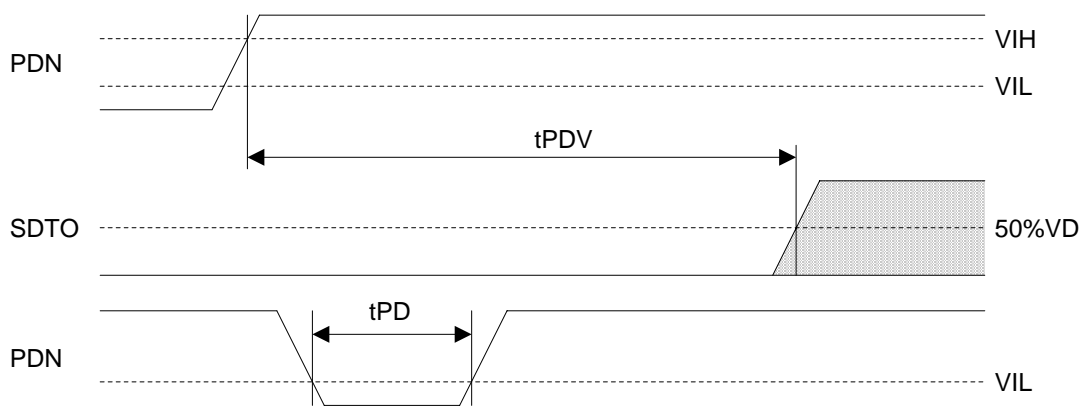
Clock Timing



Audio Interface Timing (Slave mode)



Audio Interface Timing (Master mode)



Power Down & Reset Timing

OPERATION OVERVIEW

■ System Clock

MCLK (256fs/384fs/512fs), SCLK and LRCK (fs) clocks are required in slave mode. The LRCK clock input must be synchronized with MCLK, however the phase is not critical. [Table 1](#) shows the relationship of typical sampling frequency and the system clock frequency. MCLK frequency, SCLK frequency, HPF (ON or OFF), the input level (CMOS or TTL) and master/slave are selected by CKS2-0 pins as shown in [Table 2](#).

All external clocks (MCLK, SCLK and LRCK) must be present unless the PDN pin = "L". If these clocks are not provided, the AK5357 may draw excess current due to its use of internal dynamically refreshed logic. If the external clocks are not present, place the AK5357 in power-down mode (PDN pin = "L"). In master mode, the master clock (MCLK) must be provided unless the PDN pin = "L".

| fs | MCLK | | | |
|---------|------------|------------|------------|------------|
| | 256fs | 384fs | 512fs | 768fs |
| 32kHz | 8.192MHz | 12.288MHz | 16.384MHz | 24.576MHz |
| 44.1kHz | 11.2896MHz | 16.9344MHz | 22.5792MHz | 33.8688MHz |
| 48kHz | 12.288MHz | 18.432MHz | 24.576MHz | 36.864MHz |
| 96kHz | 24.576MHz | 36.864MHz | N/A | N/A |

Table 1. System Clock Example (N/A: Not available)

| CKS2 | CKS1 | CKS0 | Input Level | HPF | Master/Slave | MCLK | SCLK | |
|------|------|------|-------------|-----|--------------|--|----------------|--|
| L | L | L | CMOS | ON | Slave | 256/384fs (~ 96kHz) 512/768fs (~ 48kHz) | ≥ 48fs or 32fs | |
| L | L | H | CMOS | OFF | Slave | 256/384fs (~ 96kHz) 512/768fs (~ 48kHz) | ≥ 48fs or 32fs | |
| L | H | L | CMOS | ON | Master | 256fs (~ 96kHz) | 64fs | |
| L | H | H | CMOS | ON | Master | 512fs (~ 48kHz) | 64fs | |
| H | L | L | TTL | ON | Slave | 256/384fs (~ 96kHz) 512/768fs (~ 48kHz) | ≥ 48fs or 32fs | |
| H | L | H | Reserved | | | | | |
| H | H | L | CMOS | ON | Master | 384fs (~ 96kHz) | 64fs | |
| H | H | H | CMOS | ON | Master | 768fs (~ 48kHz) | 64fs | |

Table 2. Mode Select

Note: SDTO outputs 16bit data at SCLK=32fs.

■ Audio Interface Format

Two kinds of data formats can be chosen with the DIF pin ([Table 3](#)). In both modes, the serial data is in MSB first, 2's complement format. The SDTO is clocked out on the falling edge of SCLK. The audio interface supports both master and slave modes. In master mode, SCLK and LRCK are output with the SCLK frequency fixed to 64fs and the LRCK frequency fixed to 1fs.

| Mode | DIF pin | SDTO | LRCK | SCLK | Figure |
|------|---------|------------------------------------|------|----------------|--------------------------|
| 0 | L | 24bit, MSB justified | H/L | ≥ 48fs or 32fs | Figure 1 |
| 1 | H | 24bit, I ² S Compatible | L/H | ≥ 48fs or 32fs | Figure 2 |

Table 3. Audio Interface Format

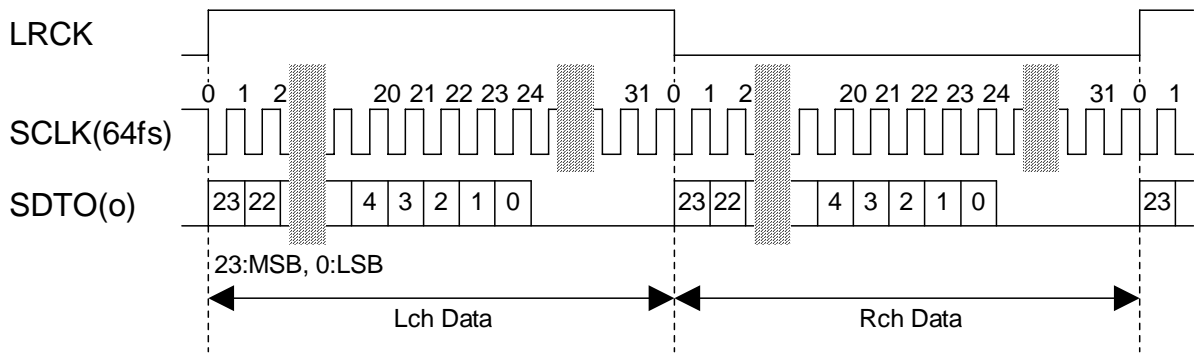


Figure 1. Mode 0 Timing

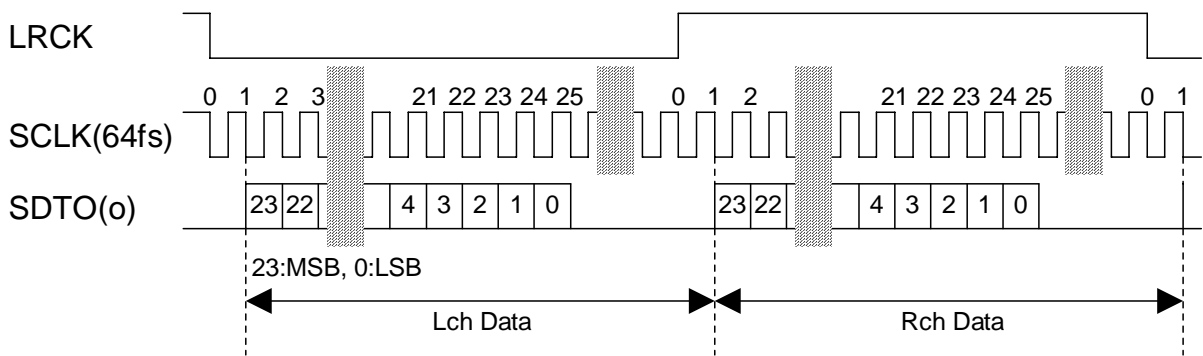


Figure 2. Mode 1 Timing

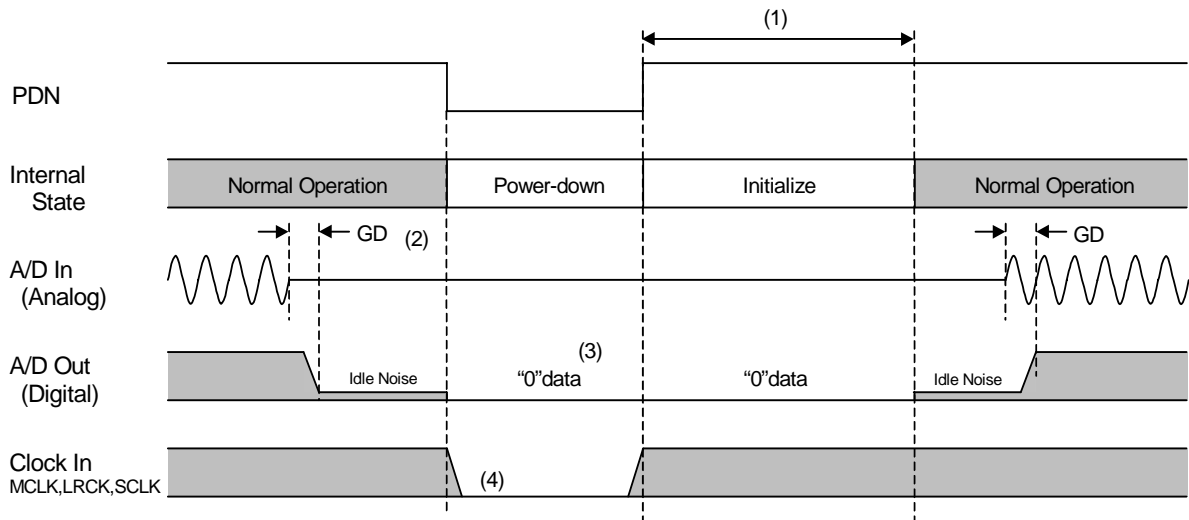
■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz (@fs=48kHz) and scales with sampling rate (fs).

HPF is controlled by CKS2-0 pins (Table 2). If HPF setting (ON/OFF) is changed when the AK5357 is in operation, click noise occurs by changing DC offset. It is recommended that HPF setting is changed when the PDN pin = "L".

■ Power down

The AK5357 is placed in the power-down mode by bringing the PDN pin “L” and the digital filter is also reset at the same time. This reset should always be executed after power-up. In the power-down mode, the VCOM is the same voltage as AGND. An analog initialization cycle starts after exiting the power-down mode. Therefore, the output data SDTO becomes available after 4129 cycles of LRCK clock in master mode or 4132 cycles of LRCK clock in slave mode. During initialization, the ADC digital output data of both channels are forced to a 2’s complement “0”. The ADC outputs settle in the value corresponding to the input signals after the initialization was completed (Settling approximately takes the group delay time).



Notes:

- (1) 4132/fs in slave mode and 4129/fs in master mode.
- (2) Digital output corresponding to analog input has the group delay (GD).
- (3) A/D output is “0” data at the power-down state.
- (4) When the external clocks (MCLK, SCLK, LRCK) are stopped, the AK5357 should be in the power-down state.

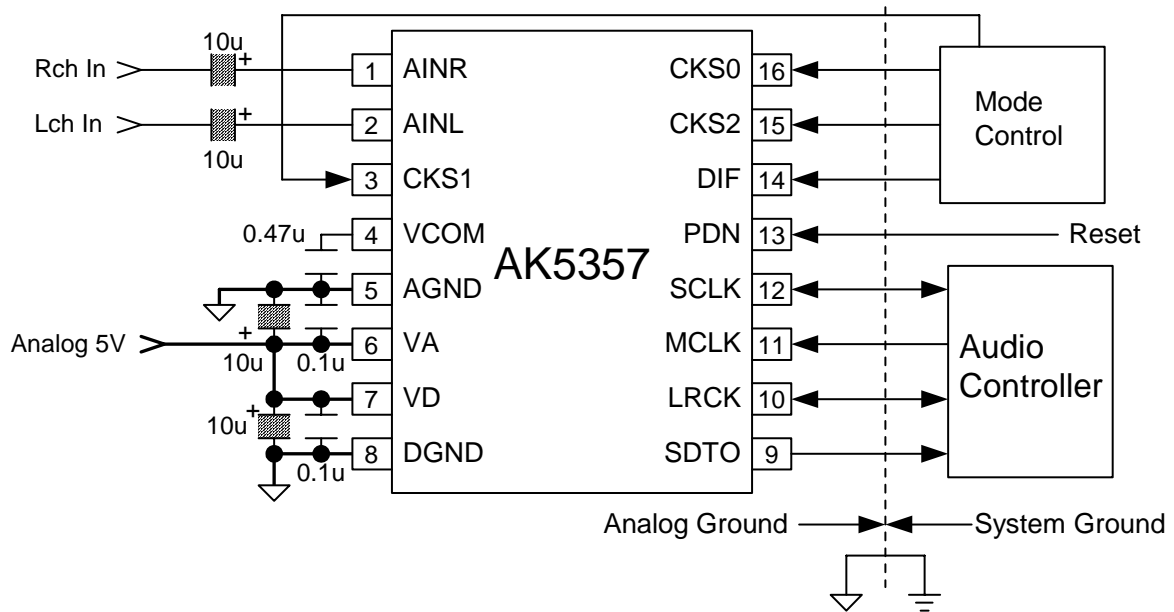
Figure 3. Power-down/up sequence example

■ System Reset

The AK5357 should be reset once by bringing the PDN pin “L” after power-up. In slave mode, the internal timing starts clocking by the rising edge (falling edge at mode 1) of LRCK after exiting from reset and power down state by MCLK. The AK5357 is power down state until LRCK is input. In master mode, the internal timing starts when MCLK is input.

SYSTEM DESIGN

Figure 4 shows the system connection diagram. The evaluation board demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.



Note:

- AGND and DGND of the AK5357 should be distributed separately from the ground of external digital devices (MPU, DSP etc.).
- All digital input pins should not be left floating.
- The CKS1 pin should be connected to VA or AGND.

Figure 4. Typical Connection Diagram

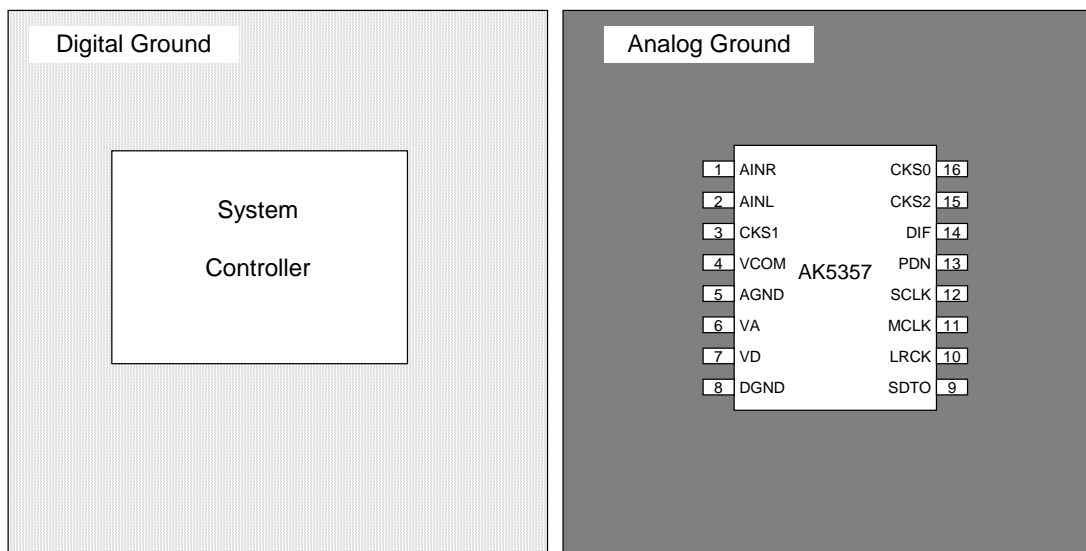


Figure 5. Ground Layout

Note:

- AGND and DGND must be connected to the same analog ground plane.

1. Grounding and Power Supply Decoupling

The AK5357 requires careful attention to power supply and grounding arrangements. Alternatively if VA and VD are supplied separately, the power up sequence is not critical. **AGND and DGND of the AK5357 must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5357 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

The voltage input to VA sets the analog input range. VCOM are 50%VA and normally connected to AGND with a 0.1 μ F ceramic capacitor. A ceramic capacitor 0.47 μ F attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from these pins. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK5357.

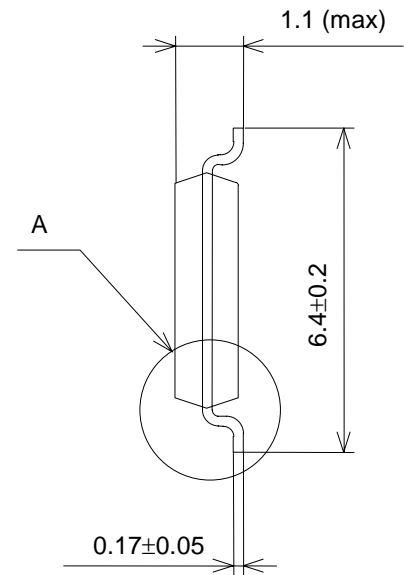
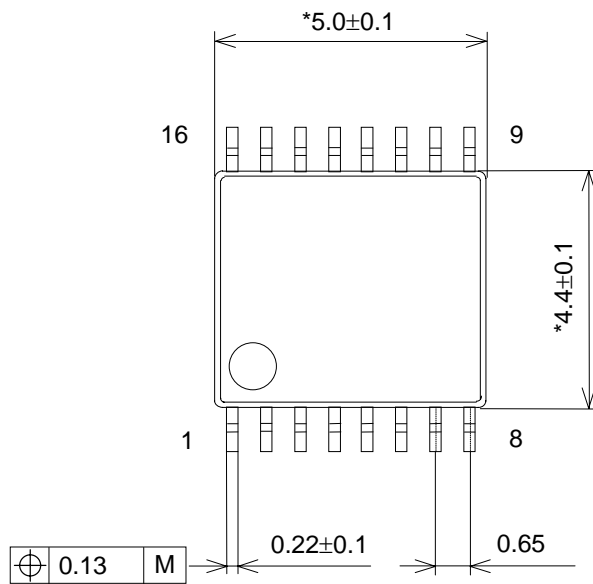
3. Analog Inputs

The ADC inputs are single-ended and internally biased to the common voltage (50%VA) with 20k Ω (typ@fs=48kHz) resistance. The input signal range scales with the supply voltage and nominally 0.6xVA Vpp (typ). The ADC output data format is 2's complement. The DC offset is removed by the internal HPF.

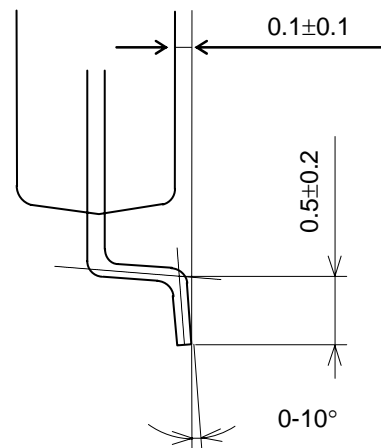
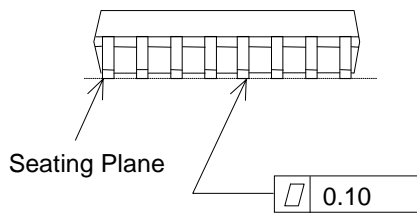
The AK5357 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. The AK5357 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

PACKAGE

16pin TSSOP (Unit: mm)



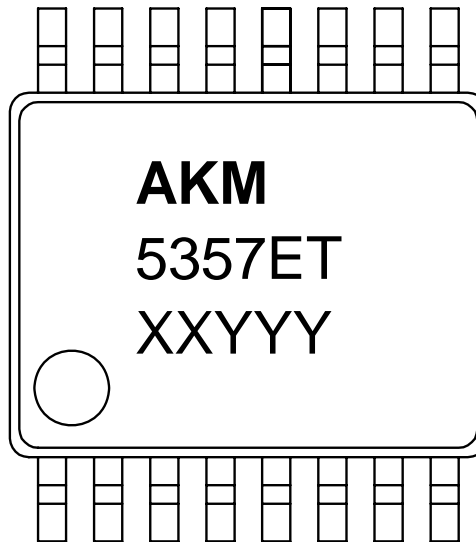
Detail A



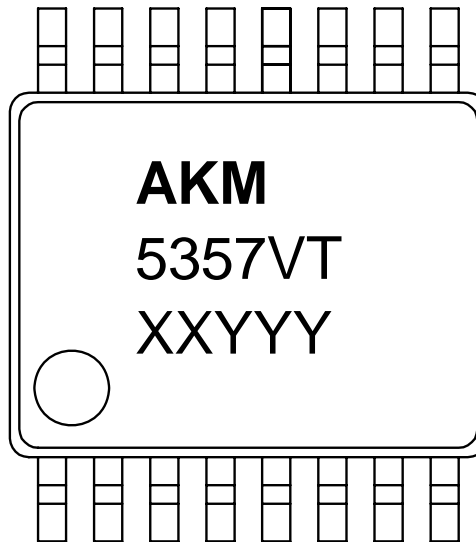
NOTE: Dimension "*" does not include mold flash.

■ Material & Lead finish

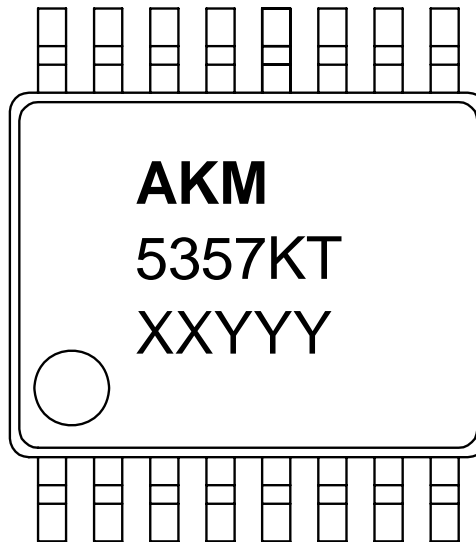
| | |
|-------------------------------|------------------------|
| Package molding compound: | Epoxy |
| Lead frame material: | Cu |
| Lead frame surface treatment: | Solder (Pb free) plate |

MARKING (AK5357ET)

- 1) Pin #1 indication
- 2) Date Code: XXYYY (5 digits)
XX: Lot#
YYY: Date Code
- 3) Marketing Code: 5357ET

MARKING (AK5357VT)

- 4) Pin #1 indication
- 5) Date Code : XYYYY (5 digits)
XX: Lot#
YYY: Date Code
- 6) Marketing Code : 5357VT

MARKING (AK5357KT)

- 7) Pin #1 indication
- 8) Date Code : XYYYY (5 digits)
XX: Lot#
YYY: Date Code
- 9) Marketing Code : 5357KT

| |
|-------------------------|
| REVISION HISTORY |
|-------------------------|

| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|-----------------|----------|------------------------|------|---|
| 04/2/24 | 00 | First Edition | | |
| 06/01/11 | 01 | Specification Addition | P.2 | Ordering Guide AK5357ET was added. |
| | | | P.18 | MARKING AK5357ET was added. |
| 07/11/22 | 02 | Specification Change | P5 | ANALOG CHARACTERISTICS of AK5357VT Input Voltage VA=5V; fs=48kHz 2.7V(min) → 2.85V(min) 3.3V(max) → 3.15V(max) |
| 09/03/27 | 03 | Product Addition | | AK5357KT (-40 ~ 105°C) was added. |

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